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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,841	12/27/2000	Balaram Sinharoy	PO9-96-134	6305

7590 03/17/2004

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	3

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/748,841	Applicant(s) SINHAROY, BALARAM
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #3. Formal Drawings as received on 4/16/2001 and #4. IDS as received on 12/27/2001.

Specification

3. The abstract of the disclosure is objected to because of the following minor informalities: In line 7, replace "contains" with --contain--. Correction is required. See MPEP § 608.01(b).

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The disclosure is objected to because of the following informalities:

For all related applications referred to within the specification, please remove the attorney docket numbers and include a U.S. application/patent number.

On page 4, line 16, replace "readonly" with --read-only-- and replace "into" with --in--.

On page 4, line 21, insert --a-- after "when".

On page 4, line 23, replace "hierarch" with --hierarchy--.

On page 4, lines 23-24, replace "I-cache replace instruction line" with --replaced I-cache instruction line--.

On page 5, line 4, replace "I-cache replace instruction line" with --replaced I-cache instruction line--.

On page 5, line 12, replace "lines" with --line--.

Replace all occurrences of "Ld_bht op" with --Ld_bht_op-- and replace all occurrences of "bht bits" with --bht_bits-- (to match Fig.1).

On page 12, line 10, should "ld_bht load" be changed to --Ld_bht_op--? The examiner has been unable to find "ld_bht load" in the figures.

On page 12, line 15, change the phrase "eight bit "branch mask" field" to --eight bit "branch mask" field (br_mask)--.

On page 12, line 17, replace "59" with --58--.

On page 13, line 19, change "replace" to --replaced--.

On page 13, line 26, insert --(FIGURE 3)-- after "201B".

On page 14, line 4, should "2047" be changed to --2048-- to correspond to 2^11?

On page 16, lines 14 and 16, branch execution logic is referred to as 214 and 211.

On page 19, line 26, insert --an-- before "IL1".

On page 20, line 7, replace "readonly" with --read-only--.

On page 25, line 3, replace "registers" with --register--.

On page 25, line 5, replace "FIGURES" with --FIGURE--.

On page 29, line 13, should "812" be changed to --810--?

On page 30, line 16, change ",," to --,--.

Insert a period at the end of line 9 on page 31.

On page 35, line 1, change "216" to --314--.

Insert a period at the end of line 2 on page 35.

On page 37, line 14, replace "1005" with --1002--.

Appropriate correction is required.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 16, reference number 214 is not shown in the drawings. On page 33, reference number 311 is not shown in the drawings. On page 36, reference number 316 is not shown in the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

In Fig.2, numbers 207, 209, 216, and 223.

In Fig.2A, numbers 206, 233, 234, and 235.

In Fig.3, numbers 304, 303, 203, 306A,B, 312, 302, 204, 207, 209, 206, 313A, 217A, 311A, and 316A,B.

Fig.5, which includes number 204, was not discussed at all in the specification.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to because of the following minor informalities: The examiner is unclear as to why, in Fig.7, that the addresses of the first instruction and first data are different in size. Shouldn't they both be 0:42 or 0:41 bits instead of them being different?

9. The drawings are objected to because of the following minor informalities: The examiner requests that Fig.8-13 be submitted in a more clear fashion. The examiner recommends putting boxes around each of the steps. This would result in much clearer figures.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

10. Claims 1-17 are objected to because of the following informalities: Please insert a colon after "comprising". Appropriate correction is required.

11. Claim 4 is objected to because of the following:

According to MPEP 608.01(m), references are enclosed within parentheses. For example in line 3 of claim 4, applicant uses "processor" to refer to "program instruction processor." Likewise, applicant uses "hit" to refer to an "access hit". However, in lines 7 and 12-13 of claim 4, the applicant appears to be trying to limit the scope of the claims through use of parentheses as opposed to establishing references. For instance, claim 4 states "...generating a hint instruction (when the instruction is a branch)...". The examiner asserts that a "when the instruction is a branch" is not an appropriate reference for a "hint instruction". Consequently, the applicant is

requested to replace the parentheses in lines 7 and 12-13 with commas, where appropriate. For purposes of this examination, the examiner will interpret the parentheses as being commas.

In addition, for increased clarity, it is recommended that the applicant remove "(instruction)" in line 5 (of claim 4) and change references to "the instruction" (for instance, lines 7 and 13) to "the program instruction".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yung, EP 0798632 A2 (herein referred to as Yung).

14. Referring to claim 4, Yung has taught a branch prediction process for a computer system for improving branch prediction rate when using a branch history table, comprising:
a) determining if a program instruction processor (processor) has an access hit (hit) or access miss (miss) in an instruction cache (I-cache) when utilizing an instruction address (IFAR address) in attempting to select a program instruction (instruction) for execution by the processor. All systems inherently have a program counter (PC / IFAR) which is used to store an instruction fetch address. This address is used to locate the current instruction by accessing the instruction cache at the IFAR address. In addition, from column 1, lines 8-16, it should be

realized that an attempt is made to access the L1 cache first. If the desired data is found, a hit occurs, and the data will be retrieved quickly. On the other hand, if the desired data is not in the L1 cache, a miss occurs, and the L2 cache is accessed.

b) generating a hint instruction (when the instruction is a branch) in response to a hit occurring during the determining operation, storing the hint instruction in association with a copy of an instruction line containing the instruction in a storage hierarchy of the computer system, the hint instruction storing BHT prediction fields obtained from a copy of a current BHT entry associated with the instruction line when the hit occurs, and storing a branch mask in the hint instruction for locating an associated BHT field (indicating the BHT field associated with the location of the instruction in the instruction line). If an I-cache hit occurs, and the current instruction is a branch, then prediction information may be generated and stored in the L1 cache. More specifically, if a branch is mispredicted, new (and hopefully more accurate) prediction information (hint instruction) will be generated and stored in the L1 cache, as implied in column 4, lines 41-51 (because the only information in a cache line that would be updated is prediction information; the instructions themselves are not changed). In addition, this hint instruction contains a BHT entry (Fig.2, fields 30 and 32), which is essentially a prediction for a particular branch instruction. Note that a BHT (branch target cache) exists within the system (column 2, lines 35-39) in order to hold prediction information (column 1, lines 46-53). Also, the hint instruction contains a branch mask (Fig.2, field 28), which specifies where the branches, and consequently, the branch predictions, are within the entry.

c) transferring the copy of the instruction line and associated hint instruction from the storage hierarchy to the I-cache in response to a miss occurring during the determining operation, and

executing the hint instruction to restore a BHT prediction field in a current BHT entry to the state of a BHT field in the hint instruction located by the branch mask. See column 2, lines 44-49, and note that when a L1 cache miss occurs, the L2 cache will be accessed and the appropriate entry with the saved hint instruction (column 2, lines 28-31) will be copied to the L1 cache such that the hint instruction is used to restore the branch prediction information for the corresponding line.

15. Referring to claim 5, Yung has taught a process as described in claim 4. Yung has further taught generating a bht index field in the hint instruction by storing an I-cache index (current I-cache index) that locates the instruction line in the I-cache and also locates the BHT entry (current BHT entry) associated with the instruction line. See Fig.2, field 26, and column 4, lines 14-15. This index field holds the address used for the entry, that is, it is the address which locates the instruction line and BHT entry with the instruction line.

16. Referring to claim 6, Yung has taught a process as described in claim 5. Yung has further taught initially providing a hint instruction no-operation code (NOP code) in the hint instruction to allocate space for a hint instruction in association with an instruction line. See Fig.3, field 44, column 4, lines 41-51, and claim 7. Note that when set to invalid, this field will specify that the branch prediction information will not be used to override a default prediction, i.e., no operation (prediction override) will occur.

17. Referring to claim 7, Yung has taught a process as described in claim 6. Yung has further taught providing a hint instruction operation code (op code) in the hint instruction to identify it as a hint instruction when fields of the hint instruction are provided. See Fig.3, field 44, column 4, lines 41-51, and claim 7. Note that when set to valid, this field will specify that

the branch prediction information will be used to override a default prediction, i.e., a prediction override operation will occur.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, as applied above, in view of Roberts, U.S. Patent No. 6,427,192.

20. Referring to claim 1, Yung has taught a branch prediction feature in a computer system for improving branch prediction rate when utilizing a branch history table (BHT) with an instruction cache, and being able to use branch history developed for instruction lines replaced in the instruction cache, comprising:

a) the instruction cache (I-cache) comprised of I-cache rows for respectively storing instruction lines fetched from a second level cache (L2 cache) in a storage hierarchy of the computer system. See column 1, lines 8-19.

b) the L2 cache comprised of L2 rows for respectively storing instruction lines fetched from a system main storage in the storage hierarchy of the computer system. See column 1, lines 8-19

c) a hint instruction location being provided in each I-cache row, and a hint instruction location being provided in each L2-cache row. See Fig.2 (L1 cache entry) and Fig.3 (L2 cache entry). Note that both entries include a hint instruction, which comprises fields 26, 28, 30, and 32 (for

Fig.2), and fields 38, 40, 42, 44,and 46 (for Fig.3). This hint instruction includes branch hints (predictions) among other things.

d) in response to an I-cache hit for a current instruction in an I-cache line, a hint processor for generating a hint instruction associated with the I-cache line, the hint instruction containing: a BHT entry and a branch mask indicating the location(s) of each branch instruction in the associated I-cache line, and a current index of the I-cache line in the I-cache, the hint processor storing the hint instruction in the hint instruction location in the current I-cache row for the current instruction. If an I-cache hit occurs, and the current instruction is a branch, then prediction information may be generated and stored in the L1 cache. More specifically, if a branch is mispredicted, new (and hopefully more accurate) prediction information (hint instruction) will be generated and stored in the L1 cache, as implied in column 4, lines 41-51 (because the only information in a cache line that would be updated is prediction information; the instructions themselves are not changed). In addition, this hint instruction contains a BHT entry (Fig.2, fields 30 and 32), which is essentially a prediction for a particular branch instruction. Note that a BHT (branch target cache) exists within the system (column 2, lines 35-39) in order to hold prediction information (column 1, lines 46-53). Also, the hint instruction contains a branch mask (Fig.2, field 28), which specifies where the branches are within the entry. Finally, the hint instruction contains a current index of the I-cache line (Fig.2, field 26).

e) in response to an I-cache miss, an L2 row containing a copy of the current I-cache instruction line and an associated hint instruction being located in the L2 cache and copied into the current I-cache row, and forwarding the hint instruction to the hint processor to be executed. See column 2, lines 44-49, and note that when a L1 cache miss occurs, the L2 cache will be accessed and the

appropriate entry with the saved hint instruction (column 2, lines 28-31) will be copied to the L1 cache such that the hint instruction is used to restore the branch prediction information for the corresponding line.

f) Yung has not explicitly taught a current BHT entry containing a prediction bit for the current instruction when the current instruction is a branch instruction, and the prediction bit being changed if the current instruction is determined to be incorrectly predicted for the current instruction. However, Roberts has taught such a concept in column 1, lines 49-55. This toggling of the prediction bit is done to try and achieve a more accurate prediction next time the branch is encountered. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yung to include such a changeable prediction bit in order to try and achieve a more accurate prediction.

21. Referring to claim 2, Yung in view of Roberts has taught a feature as described in claim 1. Yung has further taught the I-cache being located in a chip containing a central processor of the computer system (see claim 5 and Fig.5 of Yung). In addition, it is inherent that the current I-cache row is located at an I-cache index determined by a current instruction address in an instruction fetch address register (IFAR) for the current instruction being selected for execution in the chip. More specifically, all systems have a program counter (PC / IFAR) which is used to store an instruction fetch address. This address is used to locate the current instruction.

22. Referring to claim 3, Yung in view of Roberts has taught a feature as described in claim 2. Yung has not explicitly taught the I-cache being formed of two subarrays, one subarray containing a row for each instruction line in the I-cache, and the second subarray containing a row for each hint instruction in the I-cache, the I-cache index being used simultaneously in both

subarrays to locate the current instruction line in one subarray and an associated hint instruction in the other subarray. However, Yung has taught that the second level cache comprises two subarrays (see Fig.4, components 52 and 54). And from, Fig.3, it can be seen that the hint instruction is stored in the tag cache and the instructions are stored in the data cache. This is done so that each cache can be manipulated separately which is useful since the instructions are much larger than the hint instruction. See Fig.6 and column 5, lines 30-57. By having them in separate subarrays, more flexibility is gained in that one subarray can be updated while the other is read, for instance. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yung's L1 cache in a manner similar to that of Yung's L2 cache such that a more flexible access can be achieved.

23. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, as applied above, in view of Handy, "The Cache Memory Book, 2nd Edition," 1998 (herein referred to as Handy).

24. Referring to claim 8, Yung has taught a process as described in claim 4. Yung has not explicitly taught locating the copy of the instruction line in the storage hierarchy by: detecting a line address field in an I-cache directory entry associated with the instruction line in the I-cache, composing an address for the copy of the instruction line in the storage hierarchy by combining the line address field obtained by the detecting operation and an I-cache index obtained from the IFAR address of the instruction. However, Handy has taught such a concept. See page 18 and note that a tag and an index are combined to form the overall memory address. The advantage of such a design is that a set associative cache can be realized, wherein the cache takes advantage of

spatial locality by placing sequential instructions at sequential locations. This means that a processor will be able to efficiently use the cache with a less complex design because programs often execute small groups of sequential instructions. See pages 18-19 of Handy. As a result, it would have been obvious to modify Yung to include the address combination of Handy so that an efficient, less complex cache can be achieved.

25. Referring to claim 9, Yung in view of Handy has taught a process as described in claim 8. Yung has further taught accessing the copy of the instruction line and the associated hint instruction in a second level cache (L2 cache) in the storage hierarchy. See column 2, lines 44-49, and column 4, line 52, to column line 6. Note that prediction information is stored in the second level cache so that when a line is brought down from second level cache, the prediction information is restored.

26. Referring to claim 10, Yung in view of Handy has taught a process as described in claim 9. Yung has further taught storing in a main memory of the computer system a copy of the instruction line and the associated hint instruction when a L2 cache miss occurs to the storage line requiring a replacement of the storage line and the associated hint instruction in the L2 cache. See column 6, lines 6-15, and note that an alternate embodiment includes storing the victimized prediction information within main memory.

27. Referring to claim 11, Yung in view of Handy has taught a process as described in claim 10. Yung has further taught retrieving from the main memory both the copy of the instruction line and the associated hint instruction when a L2 cache miss occurs to the storage line requiring a retrieval of the storage line from the storage hierarchy. See column 1, lines 8-16. Recall from

the rejection of claim 10, that main memory is used to store victimized cache information for restoration purposes upon cache misses.

28. Referring to claim 12, Yung in view of Handy has taught a process as described in claim 9. Yung has further taught storing in a main memory of the computer system a copy of the instruction line without a copy of the associated hint instruction when a L2 cache miss occurs to the storage line requiring a replacement of the storage line and the associated hint instruction in the L2 cache to lose the hint instruction upon a L2 replacement of the instruction line. It should be noted that the first embodiment of Yung includes only storing the victimized prediction information (hint instruction) in levels of cache (not in main memory). See the abstract and column 2, lines 26-34. Consequently, if main memory needs to be accessed to retrieve a line of instructions, the prediction information will have to be restored.

29. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, as applied above.

30. Referring to claim 13, Yung has taught a process as described in claim 4. Yung has further taught the generating operation being performed by the program instruction processor for generating and executing hint instructions. Clearly, the processor 50 shown in Fig.5, will write generate branch prediction information and write it to the L1 cache. In addition, the processor 50 which accesses the hint in L1 cache, will use the hint to restore prediction information.

31. Referring to claim 14, Yung has taught a process as described in claim 4. Yung has not explicitly taught the generating operation of generating hint instructions being performed by a hint processor operating in parallel with the program instruction processor. However, Official

Notice is taken that multiprocessor systems and their advantages are well known and accepted in the art. By having multiple processors, parallelism is increased due to the fact that multiple processors work in parallel to solve a problem. Consequently, performance is increased. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a hint processor, which generates hint instructions, perform in parallel with the program instruction processor.

Allowable Subject Matter

32. Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, all objections to claims 15-17 must be overcome by applicant.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Shiell et al., U.S. Patent No. 6,108,775, has taught dynamically loadable pattern history tables in a multi-task microprocessor. More specifically, when a current task (comprising instructions) is preempted by a new task, the pattern history table entries of the current task are

also swapped with the pattern history table entries of the new task, thereby increasing efficiency by assigning each task its own prediction information.

Burrows, U.S. Patent No. 5,887,159, has taught dynamically determining instruction hint fields. Each instruction that uses a hint (including branches) is analyzed during runtime such that the best possible hint for that instruction is determined for future use.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 4, 2004

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